**4 bit ALU:-**

**implementation:**

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-- Company:

-- Engineer:

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-- Create Date: 09:53:21 05/13/2024

-- Design Name:

-- Module Name: alu\_design - Behavioral

-- Project Name:

-- Target Devices:

-- Tool versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity alu\_design is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

s : in STD\_LOGIC\_VECTOR (2 downto 0);

z : out STD\_LOGIC\_VECTOR (3 downto 0));

end alu\_design;

architecture Behavioral of alu\_design is

begin

Process(a,b,s)

begin

case s is

when "000" =>z<=a+b;

when "001" =>z<=a-b;

when "010" =>z<=a+1;

when "011" =>z<=a-1;

when "100" =>z<=a and b;

when "101" =>z<=a or b;

when "110" =>z<=a nand b;

when "111" =>z<=a nor b;

when others => null;

end case;

end Process;

end Behavioral;

**Simulation:**

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-- Company:

-- Engineer:

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-- Create Date: 10:01:02 05/13/2024

-- Design Name:

-- Module Name: /home/tib/xilinx/alu\_design/alu\_sim.vhd

-- Project Name: alu\_design

-- Target Device:

-- Tool versions:

-- Description:

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-- VHDL Test Bench Created by ISE for module: alu\_design

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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-- Notes:

-- This testbench has been automatically generated using types std\_logic and

-- std\_logic\_vector for the ports of the unit under test. Xilinx recommends

-- that these types always be used for the top-level I/O of a design in order

-- to guarantee that the testbench will bind correctly to the post-implementation

-- simulation model.

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LIBRARY ieee;

USE ieee.std\_logic\_1164.ALL;

use IEEE.STD\_LOGIC\_ARITH.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric\_std.ALL;

ENTITY alu\_sim IS

END alu\_sim;

ARCHITECTURE behavior OF alu\_sim IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT alu\_design

PORT(

a : IN std\_logic\_vector(3 downto 0);

b : IN std\_logic\_vector(3 downto 0);

s : IN std\_logic\_vector(2 downto 0);

z : OUT std\_logic\_vector(3 downto 0)

);

END COMPONENT;

--Inputs

signal a : std\_logic\_vector(3 downto 0) := (others => '0');

signal b : std\_logic\_vector(3 downto 0) := (others => '0');

signal s : std\_logic\_vector(2 downto 0) := (others => '0');

--Outputs

signal z : std\_logic\_vector(3 downto 0);

-- No clocks detected in port list. Replace <clock> below with

-- appropriate port name

--constant <clock>\_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)

uut: alu\_design PORT MAP (

a => a,

b => b,

s => s,

z => z

);

-- -- Clock process definitions

-- <clock>\_process :process

-- begin

-- <clock> <= '0';

-- wait for <clock>\_period/2;

-- <clock> <= '1';

-- wait for <clock>\_period/2;

-- end process;

-- Stimulus process

stim\_proc: process

begin

-- hold reset state for 100 ns.

a<= "1001";

b<= "0101";

s<= "000";

--wait for <clock>\_period\*10;

wait for 100 ns;

s<= "001";

-- insert stimulus here

wait;

end process;

END;

**Waveform:**

